

- 1 1. A processor comprising:
- 2 first and second instruction pointer (IP) sources to provide IPs for first and second
- 3 instruction threads, respectively;
- 4 an instruction cache to provide a cache line responsive to an IP;
- 5 a source arbiter to provide an IP from the first or second IP source to the
- 6 instruction cache;
- 7 an instruction buffer (IB) to receive a first block of the cache line; and
- 8 a temporary instruction cache (TIC) to receive a second block of the cache line.
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1 6. The system of claim 5, wherein the first IB receives an instruction block from the TIC
2 and the second IB receives an instruction block from the cache on a second clock interval.

1 7. The processor of claim 1, wherein the IB receives first and second instruction blocks
2 from the instruction cache and the TIB, respectively, on adjacent clock intervals.

1 8. The processor of claim 1, wherein the IB comprises first and second IBs and the
2 instruction cache provides instruction blocks to the first and second IBs on adjacent clock cycles.

1 9. The processor of claim 8, wherein the TIC provides instruction blocks to the first and
2 second IBs on adjacent clock cycles.

1 10. An instruction fetch engine comprising:
2 an instruction cache to provide a line of instructions in response to an instruction
3 pointer;
4 an instruction queue to receive a first block of the instruction line during a first
5 clock interval; and
6 a temporary instruction cache to receive a second block of the instruction line
7 during the first clock interval.

1 11. The instruction fetch engine of claim 10, wherein the temporary instruction cache
2 provides the second block of the instruction line to the instruction queue during a subsequent
3 clock interval.

1 12. The instruction fetch engine of claim 10, wherein the instruction cache stores lines of
2 instructions for first and second instruction threads and the instruction queue includes first and
3 second instruction queues to store blocks of instructions for the first and second instruction
4 threads, respectively.

13. The instruction fetch engine of claim 12, wherein the instruction cache provides first and
second blocks of a line of instructions for the first instruction thread to the first instruction queue
and the temporary instruction cache, respectively, during the first clock interval.

14. The instruction fetch engine of claim 13, wherein the instruction cache provides first and
second blocks of a line of instructions for the second instruction thread to the second instruction
queue and the temporary instruction cache, respectively, during a second clock interval.

1 15. The instruction fetch engine of claim 10, wherein the instruction queue includes first and
2 second instruction queues and the instruction cache provides first blocks of instruction lines for
3 the first and second instruction threads to the first and second instruction queues on alternate
4 clock intervals.

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1 16. The instruction fetch engine of claim 15, wherein the instruction queue provides second
2 blocks of the instruction lines for the first and second instruction threads to the temporary
3 instruction cache on alternate clock intervals.

1 17. The instruction fetch engine of claim 16, wherein the temporary instruction cache
2 provides the second blocks of the instruction lines for the first and second instruction threads to
3 the first and second instruction queues, respectively, on alternate clock intervals.

18. A method comprising:

selecting first and second cache lines for first and second instruction threads;

providing first and second instruction blocks of the first cache line to a first
instruction queue and a temporary instruction cache, respectively, during a first clock
interval; and

providing first and second instruction blocks of the second cache line to a second
instruction queue and the temporary instruction cache, respectively, during a second
clock interval.

1 19. The method of claim 18, further comprising providing the second block of the first cache
2 line to the first instruction queue during the second clock interval.

1 20. The method of claim 19, wherein selecting first and second cache lines comprises:

2 receiving instruction pointers for the first and second threads; and

3 providing first and second cache lines responsive to receipt of the instruction
4 pointers for the first and second threads, respectively.
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1 21. The method of claim 20, wherein receiving instruction pointers for the first and second
2 threads comprises receiving instruction pointers for the first and second threads during adjacent
3 clock intervals.

4 22. The method of claim 21, wherein providing the first and second instruction blocks
5 comprises providing the first and second instruction blocks during adjacent clock intervals.
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7 23. A system comprising:

1 1st through nth instruction pointer (IP) sources;

2 1st through nth instruction queues associated with the 1st through nth IP sources,
3 respectively;
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5 a cache to provide a first portion of an instruction block to one of the 1st through
6 4th instruction queues, responsive to an IP from the associated IP source; and

7 a temporary storage to receive a second portion of the instruction block.

